CLAIMS:

1. A network device comprising:

a device input;

at least one port;

a frequency doubler coupled to said input and configured to receive an input clock signal and output an output clock signal having double the frequency of the input clock signal;

a data I/O device and configured to output data based upon a reference clock signal; and

a programmable delay locked loop coupled to said device input and configured to receive an input signal and to automatically output an output signal being a predetermined amount out of phase from the input signal;

wherein an external clock signal received at said device input is input to said frequency doubler as the input clock signal, said output of said frequency doubler being applied to said data I/O device as a reference clock, said data being output from said data I/O device to said at least one port, said external clock signal being input to said programmable delay locked loop, said programmable delay locked loop outputting an output clock signal having a frequency equal to a frequency of the external clock signal, said output clock signal being in synchronization with said doubled clock signal.

2. The network device of claim 1, wherein said frequency doubler comprises a circuit for splitting said external clock signal into a first and

second clock signal, a delay element for delaying at least one of said first and second clock signal, and an element for integrating said first and second clock signal into said doubled clock signal.

3. The network device of claim 2, wherein said element for integrating said first and second clock signals comprises an exclusive OR gate downstream of said delay element.

4. The network device of claim 1, said network device comprising a network switch, and wherein said at least one port is configured for linking said switch to another network device.

5. The network device of claim 4, wherein said at least one port is configured to transmit and receive data at a speed of 2.5 Gbps.

6. The network device of claim 5, further comprising:

a variable delay circuit coupled to an output of said data I/O device, wherein said at least one port comprises a plurality of data pins for outputting said data in portions, a speed of said external clock signal is 156 kHz, and said variable delay circuit being applied to said data in order to prevent skew between said each portion of said data.

7. The network device of claim 6, wherein said variable delay

circuit comprises a plurality of programmable delay elements.

8. The network device of claim 1, wherein said programmable delay locked loop comprises:

a phase comparator;

a delay line comprising a plurality of variable delay elements;

a feedback loop feeding back an output of said delay line to said phase comparator;

wherein the input signal of said programmable delay locked loop is input to said phase comparator and compared to the output of said delay line, said phase comparator detecting an error between said input signal and said output of said delay line and adjusting the delay of said delay line until said error is equal to zero.

9. The network device of claim 8, wherein said plurality of delay elements include a first group of delay elements producing a first and a second delay amount, and a second group of delay elements producing a third and fourth delay amount, said first and second delay amounts being greater than twice that of said third and fourth delay amounts, respectively.

10. The network device of claim 9, wherein said phase detector increasingly delays of the output of said delay line by adjusting said first group of delay elements until a fine delay adjustment is required, then adjusting

said second group of delay elements.

11. The network device of claim 9, wherein said error is detected to be zero when said input signal and said delay line output are 90 degrees out of phase.

12. The network device of claim 1, wherein an inverter is placed between said device input and said input of said delay locked loop.

13. The network device of claim 9, wherein an inverter is placed between the device input and said input of said delay locked loop.

14. A network device comprising:

a device input means for receiving an external clock signal;

at least one port;

a frequency doubler means coupled to said device input for receiving an input clock signal and outputting a doubled output clock signal having double a frequency of the input clock signal;

a data I/O means for outputting data based upon a reference clock signal; and

a programmable delay locked loop means coupled to said device input for receiving an input clock signal and automatically outputting an output clock signal being a predetermined amount out of phase from the input signal;

wherein an external clock signal received at said device input is input to said frequency doubler means as an input clock signal, said output clock signal of said frequency doubler means being applied to said data I/O means as a reference clock, said data being output from said data I/O means to said at least one port, said external clock signal being input to said programmable delay locked loop means, said programmable delay locked loop means outputting an output clock signal having a frequency equal to the frequency of the external clock signal, said output clock signal being in synchronization with said doubled clock signal.

15. The network device of claim 14, wherein said frequency doubler means comprises a circuit for splitting said external clock signal into a first and second clock signal, a delay means for delaying at least one of said first and second clock signal, and an integration means for integrating said first and second clock signal into said doubled clock signal.

16. The network device of claim 15, wherein said integration means comprises an exclusive OR gate downstream of said delay element.

17. The network device of claim 16, said network device comprising a switch means, and wherein said at least one port is configured for linking said switch means to another network device.

18. The network device of claim 17, wherein said at least one port is configured to transmit and receive data at a speed of 2.5 Gbps.

19. The network device of claim 18, further comprising:

a variable delay circuit means coupled to an output of said data I/O device means,

wherein said at least one port comprises a plurality of data pin means for outputting said data in portions, a speed of said external clock signal is 156 kHz, and said variable delay circuit means being applied to said data in order to prevent skew between said each portion of said data.

20. The network device of claim 19, wherein said variable delay circuit means comprises a plurality of programmable delay elements.

21. The network device of claim 14, wherein said programmable delay locked loop means comprises:

a phase comparator means for detecting an error between a first and second input signal based on the phase difference between said first and second input signals;

a delay line means comprising a plurality of variable delay elements;

a feed back loop means for feeding back the output of said delay line means to said phase comparator means;

wherein the input signal of said programmable delay locked loop

means is input to said phase comparator means, said phase comparator detecting an error between said input signal and said output of said delay line means and adjusting the delay of said delay line means until said error is equal to zero.

22. The network device of claim 21, wherein said plurality of variable delay elements include a first group of variable delay elements producing a first and a second delay amount, and a second group of variable delay elements producing a third and fourth delay amount, said first and second delay amounts being greater than twice that of said third and fourth delay amounts, respectively.

23. The network device of claim 22, wherein said phase comparator means increasingly delays of the output of said delay line means by adjusting the first group of variable delay elements until a fine delay adjustment is required, then adjusting said second group of variable delay elements.

24. The network device of claim 22, wherein said error is detected to be zero when said input signal and said delay line output are 90 degrees out of phase.

25. The network device of claim 14, wherein an inverter is placed between said device input means and said input of said delay locked loop

means.

26. The network device of claim 22, wherein an inverter is placed between the device input means and said input of said delay locked loop means.

27. A method for linking network devices, said method comprising the steps of:

receiving an external clock signal at a first device;

splitting an external clock signal received by said first device into a first input clock signal and a second input clock signal;

doubling a frequency of said first input clock signal to form a doubled clock signal;

outputting data from said first device based on said doubled clock signal at double the data rate of said external clock signal, said data being outputted at a port of said first device;

delaying said data before it is outputted from said first device;

delaying said second input clock signal to be a predetermined amount out of phase with said first input clock signal; and

providing said second input clock signal to said port of said first device;

wherein said second input clock signal is delayed in order to synchronize said second input clock signal with said data, and said second

input clock signal and said data are transmitted in parallel out of said device at said port.

28. The method of step 27, further comprising the steps of:

receiving said data and said second input clock signal from an input of said second device, and sampling said data based on said second input clock signal; and

transmitting said output of said first device to said input of said second device.

29. The method of step 27, wherein said port of said device comprises a plurality of data pins for transmitting data, said method further comprising the step of:

dividing said data to be outputted into portions corresponding to each of said plurality of data pins;

variably delaying each portion of said data to synchronize said each portion of said data with one another.

30. The method of step 27, wherein said step of delaying said second input clock signal further comprises:

providing a delay locked loop comprising an input coupled to a delay line and a phase comparator, an output of said delay line being fed-back to said phase comparator;

variably adjusting said delay line until an input signal at said input is delayed out of phase based on an error signal generated by said phase comparator when said phase comparator compares the feed back from said delay line and said second input clock signal; and

outputting the delayed input signal as an output signal;

wherein said output signal is provided as said second output signal to be transmitted in parallel with said data.

31. The method of claim 27, wherein in said variably adjusting said delay line step, variably adjusting said delay line until said error signal is detected to be zero, when said input signal and said delay line output are 90 degrees out of phase.

32. A network device comprising:

a first switch comprising

an clock input for receiving an external clock signal,

a first plurality of ports,

a frequency doubler coupled to said input and configured to receive an input signal and output an output signal with a frequency which is double that of the input signal,

an I/O device configured to output data to at least one of said plurality of ports based on a first reference clock signal,

a variable delay circuit, and

a programmable delay locked loop coupled to said clock input and configured to receive an input signal and to automatically output an output signal being a predetermined amount out of phase from the input signal;

a second switch comprising

a second plurality of ports, and

a double data rate receiving unit configured to receive data and a second reference clock signal from at least one of said second plurality of ports, and to sample said data based on a rising edge and a falling edge of said second reference clock signal;

an external clock couple to said first switch; and

a circuit coupling a first link port of said first plurality of ports to a second link port of said second plurality of ports;

wherein an external clock signal received at said clock input of said first switch from said external clock is input into said frequency doubler, said output of said frequency doubler being input to said I/O device as a first reference clock signal, said I/O device outputting said data to said first link port via said variable delay circuit, said variable delay circuit delaying said data, said external clock signal also being input to said programmable delay locked loop, said output of said programmable delay locked loop being

provided to said first link port, said first switch being configured to output said data and said external clock signal from said link port in parallel to said second link port of said second switch via said circuit, said second switch being configured to receive said data and said external clock signal and to input said external clock signal as a second reference clock and said data to said double data rate receiving unit, said double data rate receiving unit sampling said data at double data rate.

33. The network device of claim 32, wherein said frequency doubler comprises a circuit for splitting said external clock signal into a first and second clock signal, a delay element for delaying at least one of said first and second clock signal, and an element for integrating said first and second clock signal into said doubled clock signal.

34. The network device of claim 33, wherein said element for integrating said first and second clock signals comprises an exclusive OR gate downstream of said delay element.

35. The network device of claim 32, wherein said first and second link ports are configured to transmit and receive data at a speed of 2.5 Gbps.

36. The network device of claim 35, wherein said first and second link port each comprise a plurality of data pins for inputting and outputting said

data in a plurality of portions, a speed of said external clock signal is 156 kHz, and said variable delay circuit being configured to delay said data in order to prevent skew between each of said plurality of portions of said data.

37. The network device of claim 32, wherein said variable delay circuit comprises a plurality of programmable delay elements.

38. The network device of claim 32, wherein said I/O device comprises a rising edge register.

39. The network device of claim 32, wherein said I/O device comprises a plurality of rising edge registers corresponding to said plurality of pins.

40. The network device of claim 32, wherein said programmable delay locked loop comprises:

a phase comparator configured to detect an error between a first and second input signal based on the phase difference between said first and second input signals;

a delay line comprising a plurality of variable delay elements;

a feedback loop for feeding back the output of said delay line to said phase comparator;

wherein the input signal of said programmable delay locked loop is

input to said phase comparator means and to said delay line, said phase comparator detecting an error between said input signal and said output of said delay line means and adjusting the delay of said delay line means until said error is equal to zero.

41. The network device of claim 40, wherein said plurality of delay elements include a first group of variable delay elements producing a first and a second delay amount, and a second group of variable delay elements producing a third and fourth delay amount, said first and second delay amounts being greater than twice that of said third and fourth delay amounts, respectively.

42. The network device of claim 41, wherein said phase comparator means increasingly delays of the output of said delay line means by adjusting the first group of variable delay elements until a fine delay adjustment is required, then adjusting said second group of variable delay elements, until said error is zero.

43. The network device of claim 41, wherein said error is detected to be zero when said input signal and said delay line output are 90 degrees out of phase.

44. The network device of claim 42, wherein an inverter is placed

between said switch input and said input of delay locked loop means.

45. The network device of claim 42, wherein an inverter is placed between the device input means and said input of said delay locked loop means.

46. A network device comprising:

a first switch means comprising

an input means,

a first plurality of ports,

a frequency doubler means coupled to said input for receiving an input signal and outputting an output signal with a frequency double that of the input signal,

an I/O device means for outputting data to at least one of said plurality of ports based on a first reference clock signal,

a variable delay circuit means, and

a programmable delay locked loop means coupled to said clock input for receiving an input signal and automatically outputting an output signal being a predetermined amount out of phase from the input signal;

a second switch means comprising

a second plurality of ports and

a double data rate receiving means for receiving data and a second reference clock signal from at least one of said second plurality of

ports, and for sampling said data based on a rising edge and a falling edge of said second reference clock signal;

an external clock means for generating an external clock signal coupled to said first switch; and

a circuit means for coupling a first link port of said first plurality of ports to a second link port of said second plurality of ports;

wherein said network device is configured such that an external clock signal received at said clock input of said first switch from said external clock means is input into said frequency doubler means, said output of said frequency doubler means being input to said I/O means as a first reference clock signal, said I/O means outputting said data to said first link port via said variable delay circuit means, said variable delay circuit means delaying said data, said external clock signal also being input to said programmable delay locked loop means, said output of said programmable delay locked loop means being provided to said first link port, said first switch means being configured to output said data and said external clock signal from said link port in parallel to said second link port of said second switch means via said circuit, said second switch means being configured to receive said data and said external clock signal and to input said external clock signal as a second reference clock and said data to said double data rate receiving means, said double data rate receiving means extracting said data at double data rate.

47. The network device of claim 46, wherein said frequency doubler

means comprises a circuit means for splitting said external clock signal into a first and second clock signal, a delay means for delaying at least one of said first and second clock signal, and an integrating means for integrating said first and second clock signal into said doubled clock signal.

48. The network device of claim 47, wherein said integrating means comprises an exclusive OR gate downstream of said delay means.

49. The network device of claim 46, wherein said first and second link ports are configured to transmit and receive data at a speed of 2.5Gbps.

50. The network device of claim 49, wherein said first and second link port each comprise a plurality of data pin means for inputting and outputting said data in a plurality of portions, said external clock means being configured to generate an external clock signal having a speed of 156 kHz, and said variable delay circuit means being configured to delay said data in order to prevent skew between each of said plurality of portions of said data.

51. The network device of claim 46, wherein said variable delay circuit means comprises a plurality of programmable delay element means.

52. The network device of claim 46, wherein said I/O means comprises a rising edge register.

53. The network device of claim 50, wherein said I/O device comprises a plurality of rising edge registers corresponding to said plurality of pins.

54. The network device of claim 46, wherein said programmable delay locked loop comprises:

a phase comparator means for detecting an error between a first and second input signal based on the phase difference between said first and second input signals;

a delay line means for variably delaying of a signal comprising a plurality of variable delay means;

a feedback loop means for feeding back the output of said delay line means to said phase comparator means;

wherein the input signal of said programmable delay locked loop means is input to said phase comparator means and to said delay line means, said phase comparator means detecting an error between said input signal and said output of said delay line means and adjusting the delay of said delay line means until said error is equal to zero.

55. The network device of claim 54, wherein said plurality of delay means include a first group of variable delay elements producing a first and a second delay amount, and a second group of variable delay elements

producing a third and fourth delay amount, said first and second delay amounts being greater than twice that of said third and fourth delay amounts, respectively.

56. The network device of claim 55, wherein said phase comparator means increasingly delays of the output of said delay line means by adjusting the first group of variable delay elements until a fine delay adjustment is required, then adjusting said second group of variable delay elements.

57. The network device of claim 56, wherein said error is detected to be zero when said input signal and said delay line means output are 90 degrees out of phase.

58. The network device of claim 56, wherein an inverter is placed between said switch input and said input of delay locked loop means.

59. The network device of claim 56, wherein an inverter is placed between the device input means and said input of said delay locked loop means.